Investigating the incomplete transition of H1 and H2 clock signals in the A3025 HBCAM main boards

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Introduction

The A3025 HBCAM circuit board, whose schematic is identical to the A2075 found here, is designed to support two external ICX424 image sensors. Detailed information regarding the purpose and operation of the HBCAM can be found in the BCAM User Manual. The ICX424 image sensor is a charge-coupled device (CCD) composed of an epitaxial layer of silicon and a shift register. The silicon acts as a photoactive layer composed of a capacitor array, a 692×504 array for the ICX424, that absorbs light. The capacitors store light shined at each location as electric charge proportional to the intensity of light. The shift register proceeds to transfer the charges by shifting all the charges one row down, the bottom-most row being the output row. Two clock signals, $H1$ and $H2$, provided by the programmable logic chip in the A3025 alternate between two logic levels: a low of 0 and a high of 3.5V. They are used to shift charges in the output row horizontally whose right-most charge is dumped into a charge amplifier that converts its charge into a voltage. Once the output row is empty, the charges are again shifted down a row, and the process repeats. The result is $692 \times 504 = 348,768$ voltages that are processed and interpreted as a 692×504 pixel image. Figure 1 shows a picture of a completed ICX424 Minimal Head circuit board (A2076).

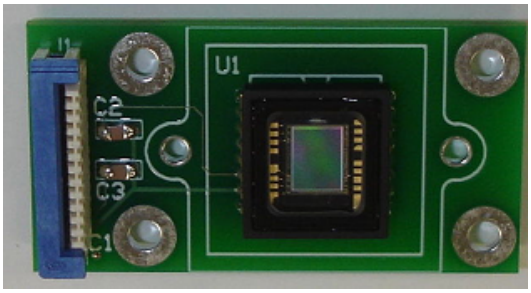


Figure 1: A2076 circuit board with the ICX424 image sensor attached (U1). [1]

The clock signals $H1$ and $H2$ are amplified by a non-inverting operation amplifier (LM6172 op-amp), powered by a 30 volt power supply. The schematic of the op-amp is shown in Figure 2. The feedback resistor, R_f, has a resistance of 1000 Ω and the ground resistor, R_g, has a resistance of 2200 Ω. It is important to note that $H2$ is an inverted signal of $H1$—its logic level is the opposite at any given time. This is because a transition from both high to low and low to high is necessary to trigger the horizontal transfer of charges in the output row. Two standard $H1$ clock pulses of the output of the op-amp, V_{out}, for the A3025 board are shown in Figure 3a with no image sensors attached. The voltage measured at V_{out}, approximately 5V, is in accordance to the theory of non-inverting amplifiers,[1] where

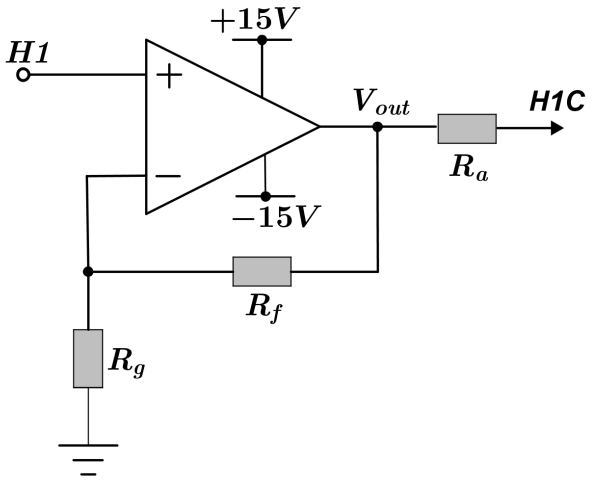


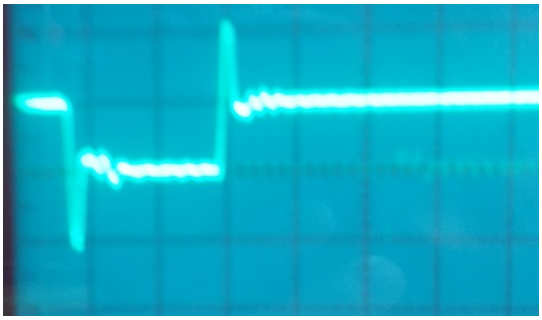
Figure 2: Schematic of the non-inverting amplifier.

$$V_{out} = V_{in}\left(1 + \frac{R_f}{R_g}\right). \tag{1}$$

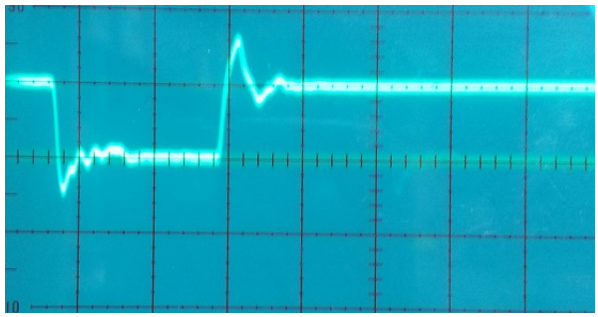
However, we see a large overshoot when measuring the voltage at the output of the op-amp because in

[1] See Appendix for background on op-amps.

practice the op-amp does not have infinite gain, resulting in a delay between the actual voltage level and its output. To account for this, we introduce a resistor, R_a, placed directly after its output. The resultant



(a) V_{out} with no ICX424 image sensors attached.



(b) $H1C$ with $R_a = 47\ \Omega$ and no ICX424 image sensors attached.

Figure 3: Vertical axis: 5V/div; Horizontal axis: 50ns/div; 0 volt line centered with vertical tick marks.

signal that is sent to the image sensor, $H1C$, is slightly attenuated and has less overshoot, as seen in Figure 3b. The resistor is even more effective with the addition of image sensors since they introduce a capacitance, resulting in a series RC load.

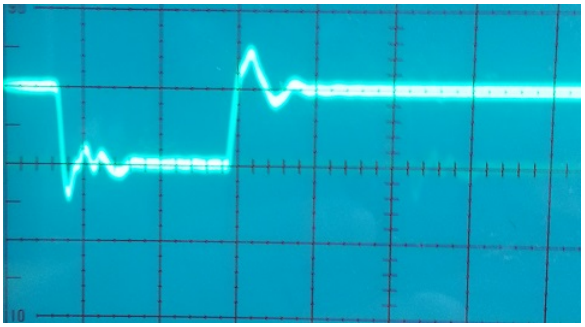
Capacitance in the image sensor

Each image sensor has a capacitance between horizontal transfer clocks and the ground of 47 pF. Thus combined with the resistor placed after the output, we have effectively created a series RC circuit. Assuming the circuit is connected to a DC voltage source at time $t = 0$, the voltage across the capacitor ideally evolves exponentially as

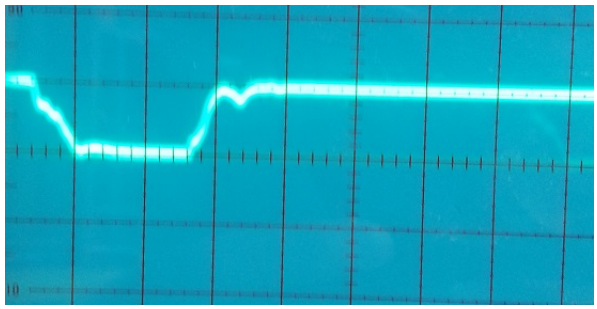
$$V_C(t) = V_{in}\left(1 - e^{-t/RC}\right). \tag{2}$$

We can think of the transition between logic levels as such a switch, from which we can see that the time it takes the capacitor to charge and discharge is the limiting factor in the horizontal clocking. We see from equation (2) that the time is related to the product of RC; this product is known as the RC time constant. The time it takes for the voltage to reach $1/e \approx 0.37$ of its original value, or equivalently decrease by $\approx 63\%$, is equal to RC.

This exponential behavior as the capacitor charges and discharges is shown in Figure 4 with two image sensors attached, most notably in $H1C$. The low and high logic signals alternate for 125 nanoseconds and



(a) V_{out} with two ICX424 image sensors attached



(b) $H1C$ with $R_a = 47\ \Omega$ and two ICX424 image sensors attached

Figure 4: Vertical axis: 5V/div; Horizontal axis: 50ns/div; 0 volt line centered with vertical tick marks.

375 nanoseconds, respectively. In this particular case, the RC time constant with two image sensors is

$$RC = 94\,\text{pF} \cdot 47\,\Omega = 4418\,\text{ps} \approx 4.4\,\text{ns}.$$

Evidently, the image sensor does not act as a perfect capacitor since the voltage decreases at a slower than expected rate. Proof of this is seen on the oscilloscope reading in Figure 5 that shows voltages measured at $H1C$ where the image sensors have been replaced with a 100 pF capacitor, resulting in a 47 Ω resistor in series with a 100 pF capacitor. Here we see the rapid transition between logic levels based upon the RC time constant calculated above.

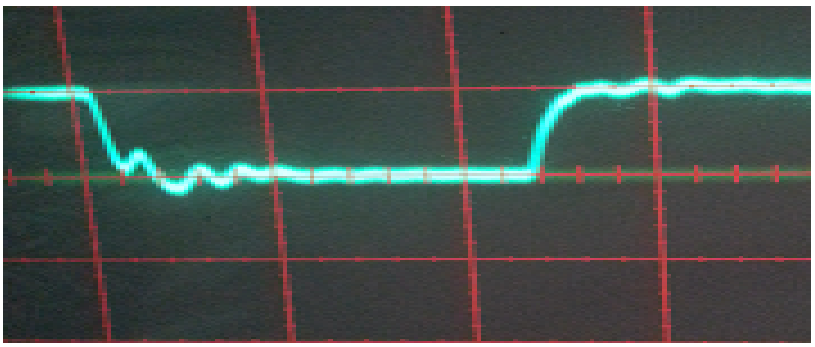
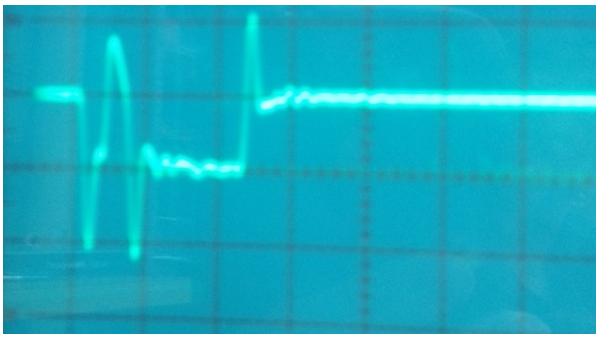


Figure 5: $H1C$ with a 47 Ω resistor in series with a 100 pF capacitor. Vertical axis: 5V/div; Horizontal axis: 50ns/div; 0 volt line centered.

Quadruple pixel setting

The ICX424 can also be set to combine pixels, converting 2×2 arrays into one large pixel; this setting is known as the ICX424Q and acts very similarly.[2] The shift register shifts charges down *two* rows at each step, resulting in two output rows, as opposed to only one in the ICX424. The charges are binned into a 2×2 array, whose information becomes a superposition of the four original charges and is interpreted and stored as only one pixel. This creates an image with a quarter of the pixels and allows for transmission over the internet at quadruple the speed. A horizontal clocking with two pulses, as seen in Figure 6, is needed to shift a block of 2×2 charges into the charge amplifier. For $H1C$, the first pulse consists of a 25



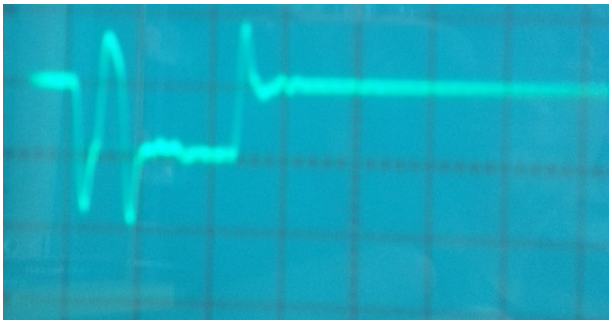


Figure 6: V_{out} (left) and $H1C$ (right) with $R_a = 47$ Ω and no ICX424Q image sensors attached. Vertical axis: 5V/div; Horizontal axis: 50ns/div; 0 volt line centered with vertical tick marks.

ns low followed by a 25 ns high, and the second pulse consists of a 75 ns low followed by a 375 ns high.

The incomplete transition in the ICX424Q

The attachment of two image sensors results in an incomplete transition of the first low-high pulse measured at $H1C$ after attenuation from the resistor, as seen in Figure 8. This problem does not arise when only one image sensor is attached, as seen in Figure 7, due to a doubling of capacitance with both attached. In order to complete the transition between logic levels, it is necessary to decrease the resistance of R_a; we see this clearly in V_{out}, before the voltage has been attenuated by a resistor. Replacing both 47 Ω resistors with 10 Ω resistors yields nicer, though far from perfect, results, as shown below in Figure 9.

As mentioned earlier, both $H1$ and $H2$ are necessary components of the horizontal clocking and we are interested in their simultaneous behavior. Figure 10 examines the difference between clock signals, $(H1C - H2C)$, with $R_a = 10$ Ω for both the ICX424 and the ICX424Q. The transition between logic levels

[2]While the image sensor itself is still the ICX424, we refer to the quadruple pixel setting as the ICX424Q for brevity.

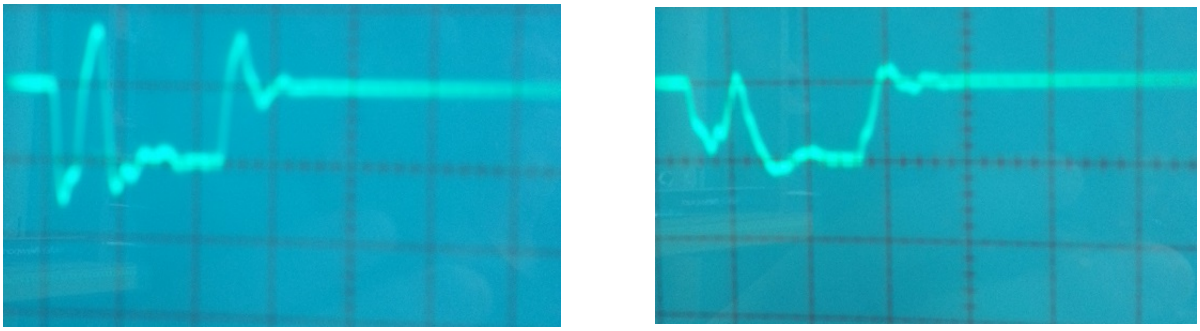


Figure 7: V_{out} (left) and $H1C$ (right) with $R_a = 47\ \Omega$ and one ICX424Q image sensor attached.
Vertical axis: 5V/div; Horizontal axis: 50ns/div; 0 volt line centered with vertical tick marks.

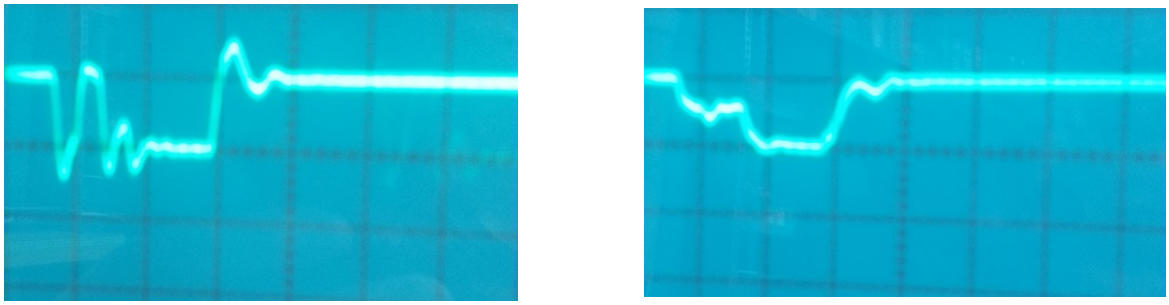


Figure 8: V_{out} (left) and $H1C$ (right) with $R_a = 47\ \Omega$ and two ICX424Q image sensor attached.
Vertical axis: 5V/div; Horizontal axis: 50ns/div; 0 volt line centered with vertical tick marks.

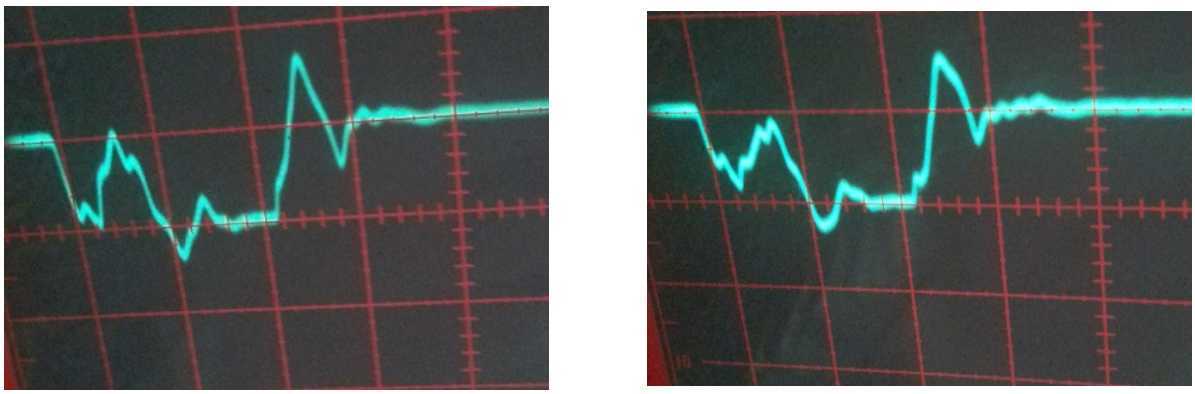


Figure 9: V_{out} (left) and $H1C$ (right) with $R_a = 10\ \Omega$ and two ICX424Q image sensors attached.
Vertical axis: 5V/div; Horizontal axis: 50ns/div; 0 volt line centered with vertical tick marks.

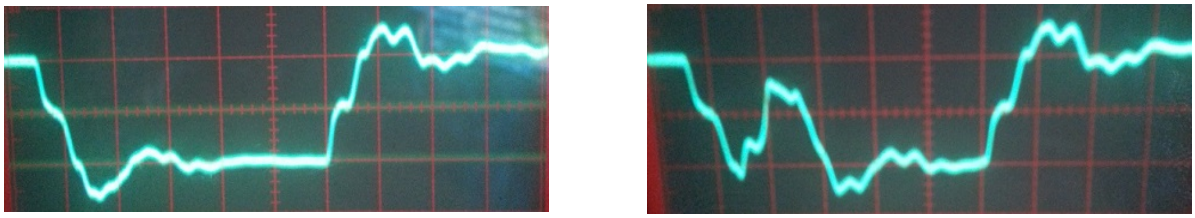


Figure 10: $(H1C - H2C)$ with $R_a = 10\ \Omega$ for the ICX424 (left) and the ICX424Q (right).
Vertical axis: 5V/div; Horizontal axis: 20ns/div; 0 volt line centered with vertical tick marks.

is most questionable with the attachment of two images sensors, as the capacitance is greatest, and from this point onwards, all oscilloscope measurements and images will assume the attachment of two image

sensors unless otherwise stated.

Supposing two perfect H1C and H2C signals, one where there is no overshoot and delayed transitions between logic levels, we expect a 125ns −5V low followed by a 375ns +5V high for the ICX424; we see the general shape with a slight overshoot in Figure 10. For the ICX424Q, we expect a 25ns −5V low followed by a 25ns +5V high for the first pulse, and then a 75ns −5V low followed by a 375ns +5V high for the second pulse. This idealization for the ICX424Q is shown to the right in Figure 11. The measurement of the ICX424Q is less promising, as the high of the first pulse barely reaches +3V.

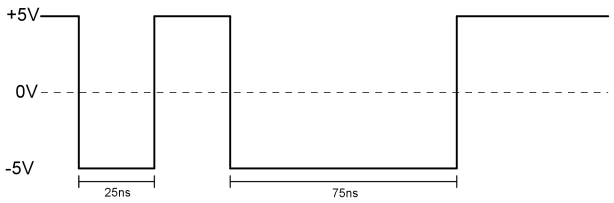


Figure 11: Ideal ICX424Q ($H1C - H2C$) signal.

Functionality of an incomplete transition

In order to test whether a transition from −5V to +3V is sufficient to trigger the horizontal clocking, we must examine the images produced by the ICX424Q. We took a series of test images with various resistances of R_a ranging from 0 Ω to 200 Ω for both the ICX424 and the ICX424Q. Figures 12 and 13 show images of black and white stripe patterns taken by the ICX424 (resized to match its quadruple pixel counterpart) and ICX424Q respectively, with no resistance and $R_a = 10$ Ω.

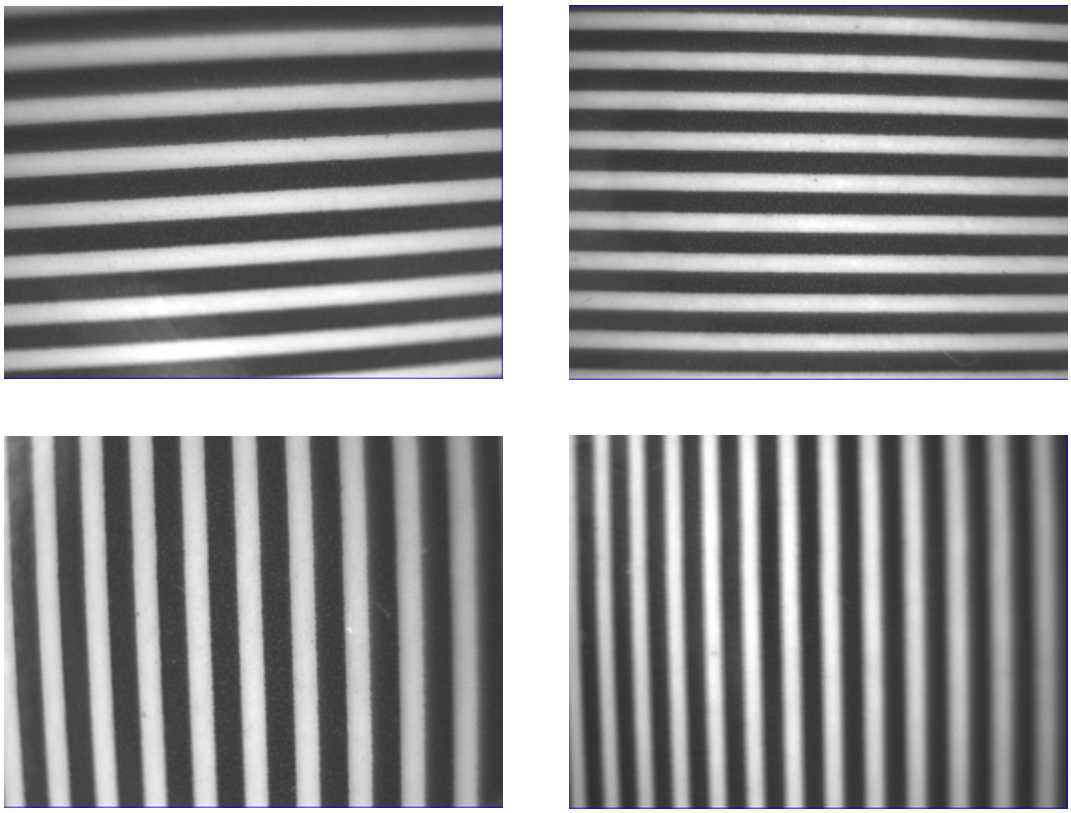


Figure 12: ICX424 test images comparing image quality with no resistor (left) and $R_a = 10$ Ω (right).

We expect distortions in the image if the horizontal clock signals not are transmitted properly, and thus the horizontal movement of charges in the output row functions abnormally. We do not see these distortions with $R_a = 10$ Ω for either image sensor setting, which suggests that the transition from −5V to +3V is enough to trigger the horizontal clocking. To strengthen this hypothesis, we gradually increased the resistance of R_a and took test images with a 22 Ω, 47 Ω, 100 Ω, and 200 Ω resistor. The images taken

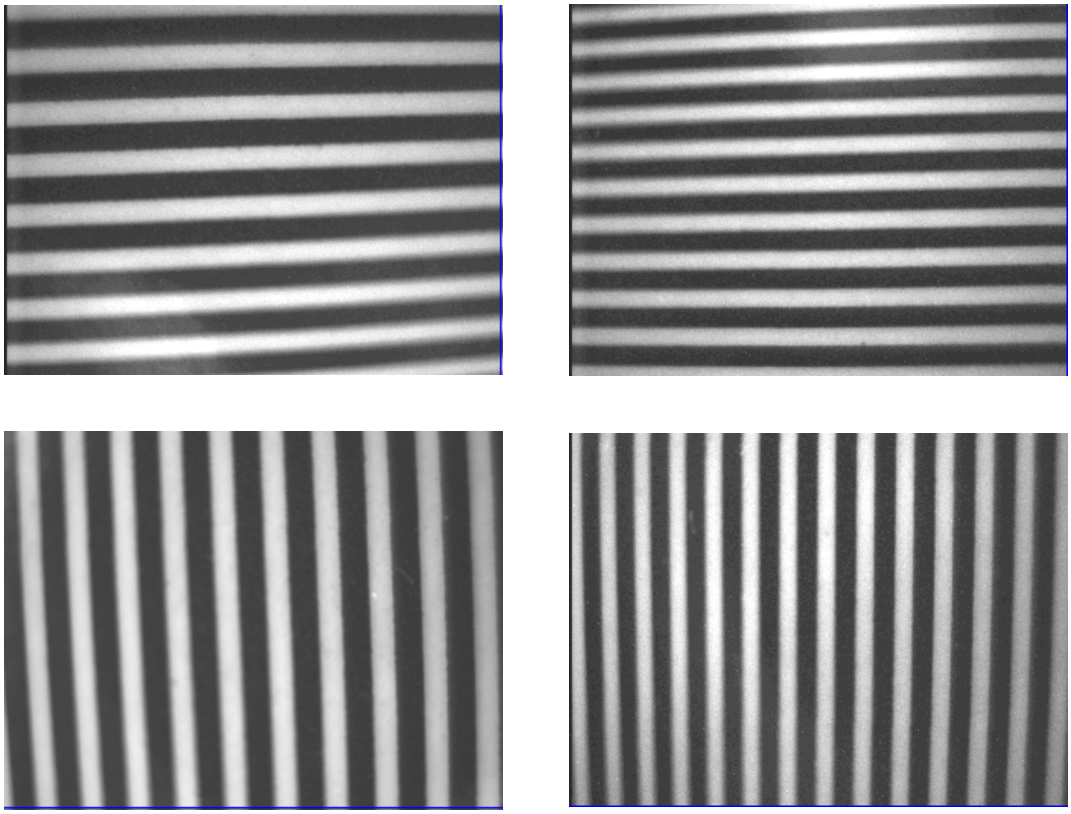


Figure 13: ICX424Q test images comparing image quality with no resistor (left) and $R_a = 10\ \Omega$ (right).

with $R_a = 22\ \Omega$ and even $R_a = 47\ \Omega$ seem promising as well, as seen in Figure 14.[3]

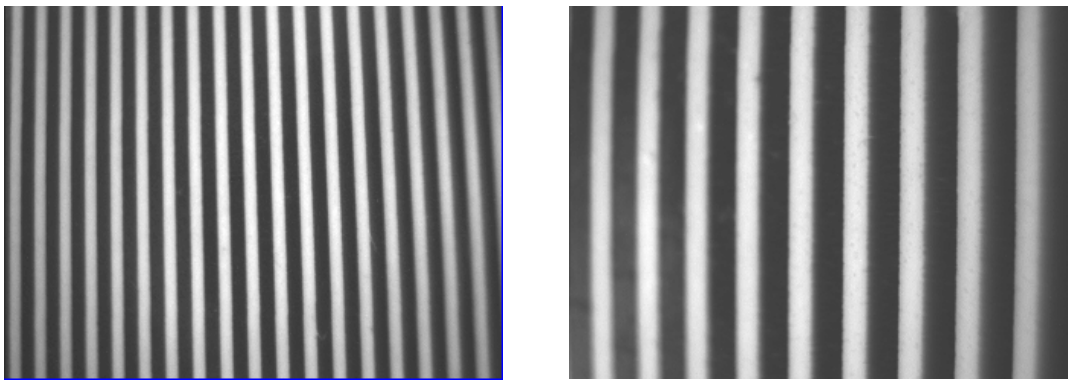


Figure 14: ICX424Q test images with a $R_a = 22\ \Omega$ (left) and $R_a = 47\ \Omega$ (right).

The image quality begins to break down at 100 Ω for the quadruple pixel setting as seen in Figure 15. The column on the left displays images taken by the ICX424 that show no distortions, unlike those taken by the ICX424Q in the column on the right.

An examination of clock signals is consistent with these results; oscilloscope readings for both image sensor settings are displayed in Figure 16. The transition from −5V to −5V is present in the ICX424, whereas the first pulse for the horizontal clocking in the ICX424Q barely reaches a low of 0V and a high of +3V, as opposed to the expected −5V to +5V. Doubling the resistance to 200 Ω worsens the transition, and the expected low of −5V is instead measured to be +2V as seen in Figure 17. The one pulse in the ICX424, however, still manages to achieve a low of −4V and rebounds to a high of +5V. Test images with

[3]For test images of horizontal stripes, see the Additional Images section.

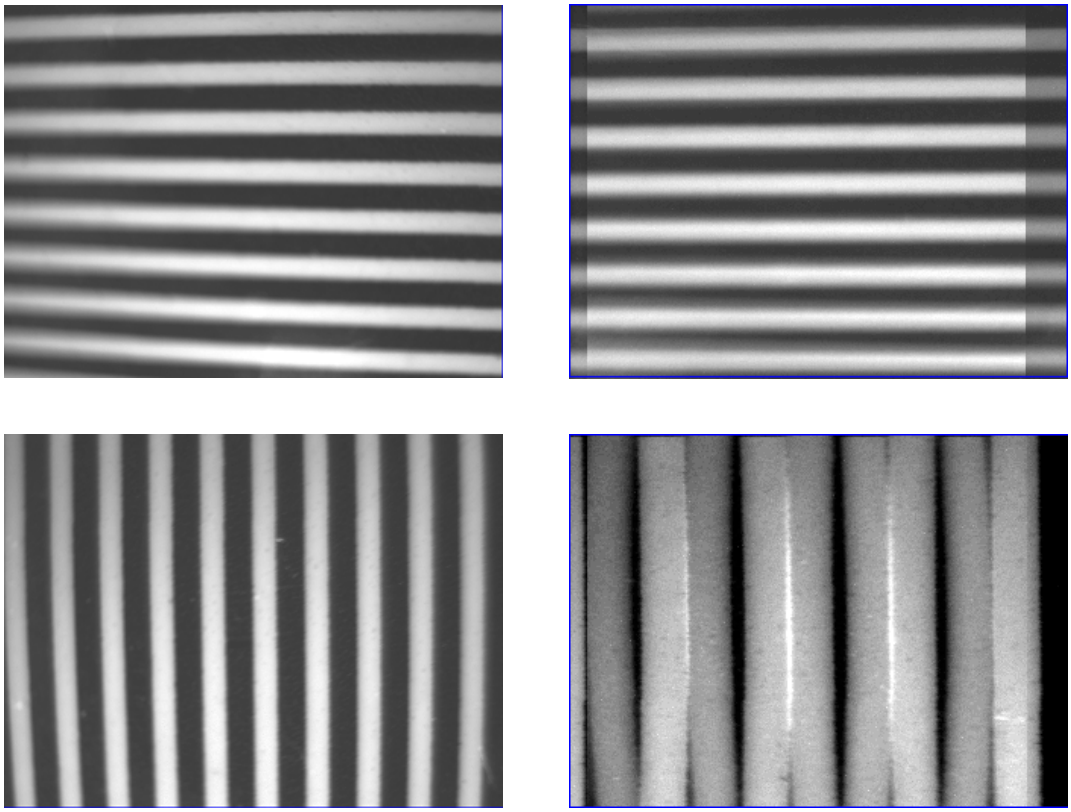


Figure 15: Test images taken by the ICX424 (left) and the ICX424Q (right) with a $R_a = 100\ \Omega$. We begin to see distortions for the ICX424Q.

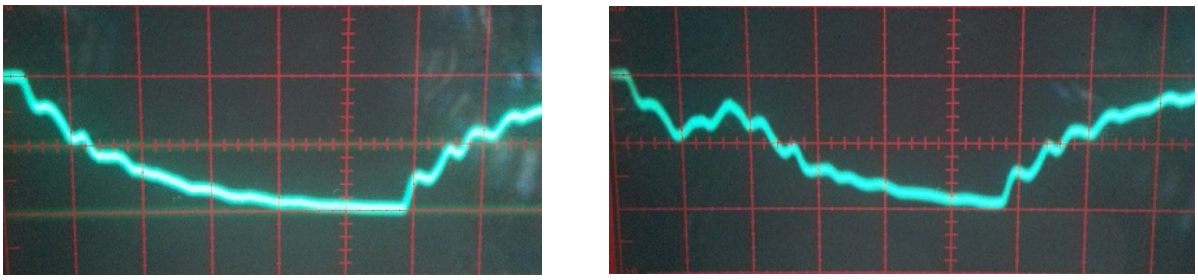


Figure 16: $(H1C - H2C)$ with $R_a = 100\ \Omega$ for the ICX424 (left) and the ICX424Q (right).
Vertical axis: 5V/div; Horizontal axis: 20ns/div; 0 volt line centered with vertical tick marks.

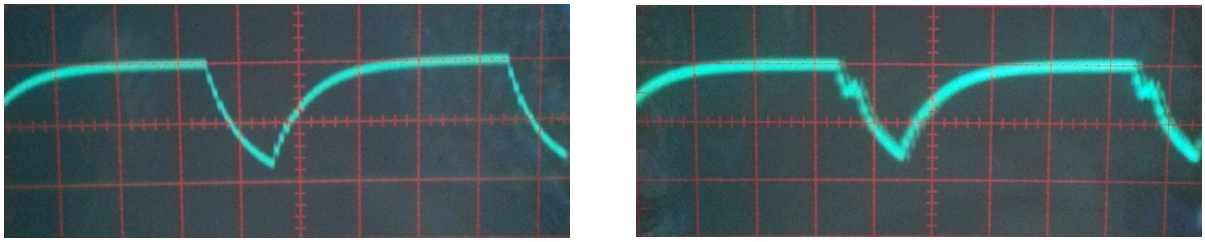


Figure 17: $(H1C - H2C)$ with $R_a = 200\ \Omega$ for the ICX414 (left) and the ICX424Q (right).
Vertical axis: 5V/div; Horizontal axis: 100ns/div; 0 volt line centered with vertical tick marks.

a 200 Ω resistor for the ICX424 show no distortions, as opposed to the ICX424Q; this is seen in Figure 18. The distortion on the quadruple pixel setting is evident in an image of a person as well, seen in Figure 19.

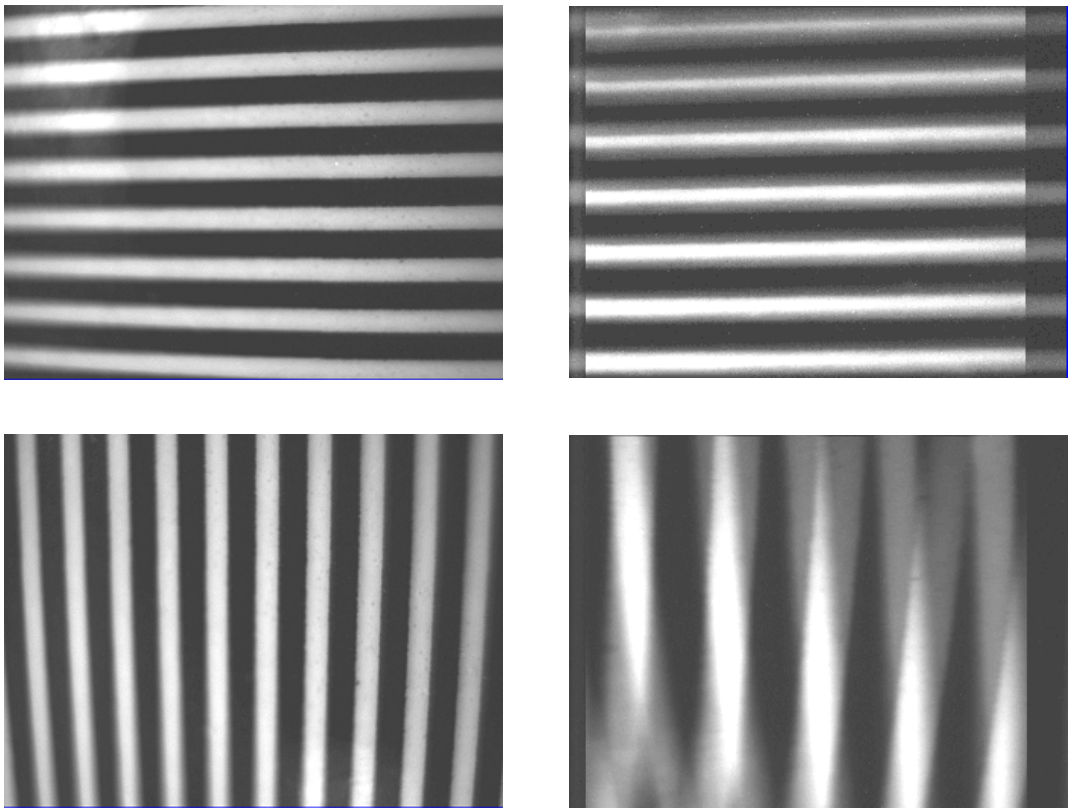


Figure 18: Test images taken by the ICX424 (left) and the ICX424Q (right) with $R_a = 200\ \Omega$. The ICX424 still shows no signs of distortion.

Figure 19: Distortion seen in an image taken by the ICX424Q with $R_a = 200\ \Omega$.

Further accounting for overshoot

Because of the relatively small resistance used in order to ensure the successful transition between logic levels, the overshoot is noticeable. In an attempt to minimize this while still maintaining a functional

horizontal clocking, we introduce a capacitor in parallel with the feedback resistor in the feedback loop of the op-amp. Assuming an initially uncharged feedback capacitor, it can be shown that the resultant output of the op-amp, H1C, as a function of time becomes[4]

$$V_{out}(t) = V_{in}\left(1 + \frac{R_f}{R_g}\right)\left(1 - e^{-t/R_f C}\right), \tag{3}$$

where R_f is the feedback resistor, R_g is the ground resistor, and C is the capacitance of the feedback capacitor. The output voltage is not amplified immediately, unlike a pure non-inverting amplifier (equation 1), but rather increases at a rate dictated by the product $R_f C$. The schematic is shown to the right in Figure 20. An initially uncharged capacitor suddenly connected to a DC source mimics a transition from a low logic level to a high, and it can also easily be shown that the output voltage of a transition from high to low, representing an initially charged capacitor with no external DC source, is simply

$$V_{out}(t) = V_{in}\left(1 + \frac{R_f}{R_g}\right)e^{-t/R_f C}. \tag{4}$$

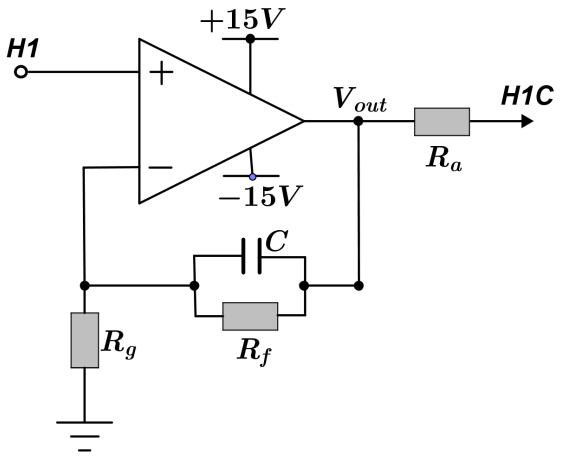


Figure 20: Schematic of the non-inverting amplifier with an additional feedback capacitor.

In choosing a capacitor fit for the job, we must consider the time intervals between logic level transitions. For the ICX424Q, a successful transition must be made in 25 ns. With a feedback resistor of 1000 Ω, a capacitor with capacitance 10 pF yields an RC time constant of 10 ns. In practice, however, a slightly higher capacitance is necessary to combat the overshoot produced by a non-ideal op-amp. An oscilloscope reading of $(H1C - H2C)$ with a 15 pF feedback capacitor is shown in Figure 21, with associated stripe test images in Figure 22.

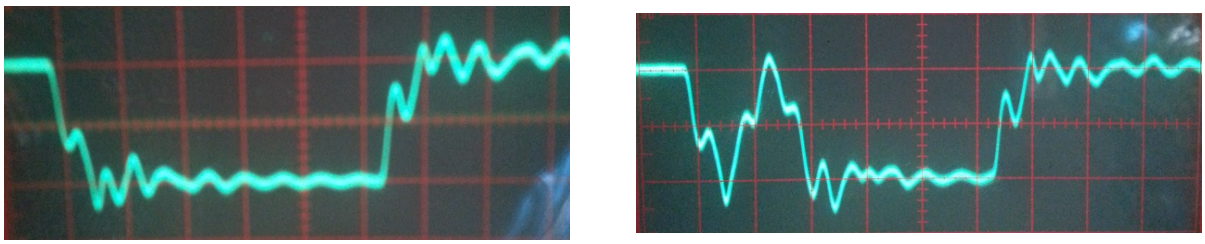


Figure 21: $(H1C - H2C)$ with $R_a = 10\ \Omega$ and $C = 15$ pF for the ICX424 (left) and the ICX424Q (right). Vertical axis: 5V/div; Horizontal axis: 20ns/div; 0 volt line centered with vertical tick marks.

Conclusions

The stripe test images suggest that it is sufficient to trigger the horizontal clocking when there is a sign change in $(H1C - H2C)$, and that only a difference in the sign of the potential is required to shift the charges in the image sensor. This sign difference with small overshoot can be achieved solely by placing a 10 Ω resistor after the output of the op-amps that, combined with the capacitive load created by the image sensors, attenuates the voltage reaching the images sensors slightly. However, introducing a feedback capacitor in parallel with the feedback resistor of the op-amp manages to reduce the overshoot further and *improves* the transition between logic levels. Figure 21 demonstrates successful transitions to ±5V made within the time frame required, with minimal overshoot. Stripe test images of this configuration also yield

[4]See Appendix for derivation.

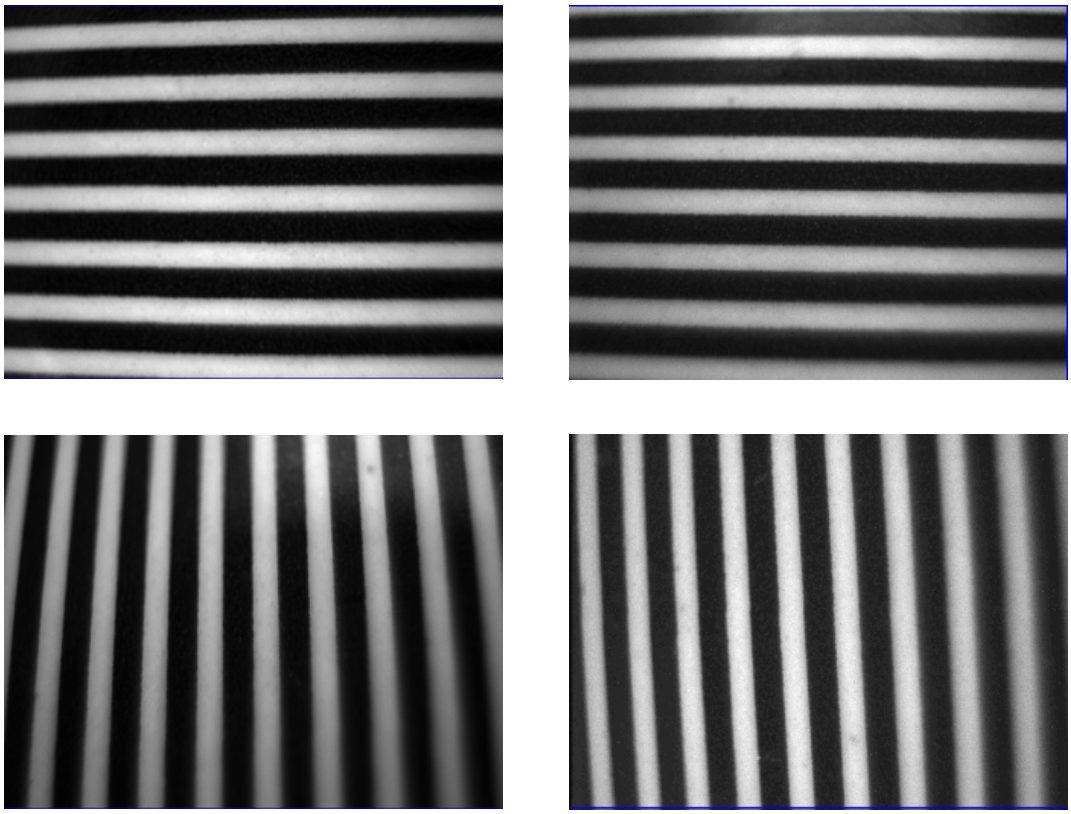


Figure 22: Test images taken by the ICX424 (left) and ICX424Q (right) with $R_a = 10\ \Omega$ and $C = 15$ pF.

images that show no signs of distortion. Thus, it seems that this is the optimal configuration to achieve confidence in the quality of the images taken by the ICX424 image sensors on its normal and quadruple pixel setting.

Final considerations and proposed changes

In the process of troubleshooting and testing the A3025 HBCAM boards, many logic chips were destroyed by the probing of an oscilloscope. The logic chip would be damaged when pins 3 and 4 of the op-amp in question, marked U7 on the schematic, were shorted, causing current to flow freely from the -15V power supply to the non-inverting input, and then back to the logic chip. In an effort to protect the logic chip from an accidental short, we introduce a resistor, R_p, directly before the non-inverting input so that the current that would flow from the power supply is drastically reduced. This addition mimics a series RC load with the resistor and the input capacitance of the op-amp, so the resistance of R_p must be chosen such that the non-inverting input reaches its desired value of 3.5V within 25 ns. A resistance of 500 Ω manages to protect the logic chip with a slightly smoother signal at the cost of slight undershoot, as seen in an oscilloscope reading of H1C in Figure 23 to the right. This smoothing effect removes unexpected jumps in voltages and should also be implemented for H2C, despite there being no danger of shorting its input to the power supply.[5] One way to counteract the undershoot is to remove the resistor placed

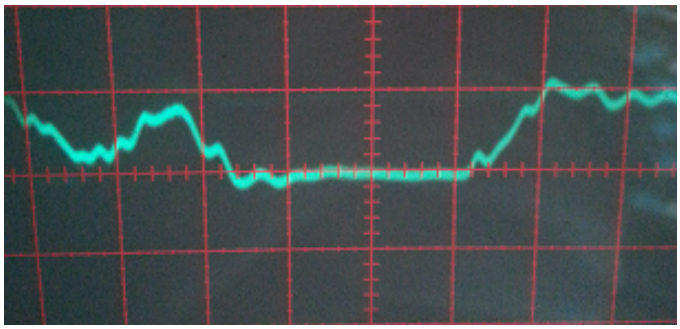


Figure 23: $H1C$ with $R_p = 500\ \Omega$, $R_a = 10\ \Omega$, $C = 15$ pF. Vertical: 5V/div; Horizontal: 50ns/div.

[5] A resistor of 510 Ω ($\pm 5\%$) was used for $H2$, but two 1000 Ω ($\pm 5\%$) resistors in parallel were used for $H1$.

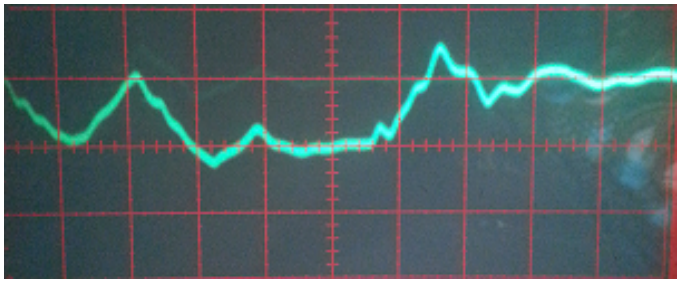


Figure 24: $H1C$ with $R_p = 500\ \Omega$, $R_a = 0\ \Omega$, $C = 15$ pF.
Vertical axis: 5V/div; Horizontal axis: 20ns/div; 0 volt line centered with vertical tick marks.

directly after the op-amp output, R_a, resulting in a signal as shown in Figure 24. In fact, it is favorable to remove R_a on all op-amps that have such a resistor since $H1C$ and $H2C$ are properly transmitted, the overshoot on the signal RC is not a problem, especially combined with the feedback capacitor, and VL reaches its intended -7.7 V with no issues. Referring to this schematic, the resistor R_a refers to R40, R41, R42, and R43. Removing those four resistors allows for one fewer component, protects the lattice chip and most importantly, yields promising clock signals and images, as shown in Figures 25 and 26. The addition of the 500 Ω resistor results in clock signals that barely overshoot when one or no image sensors are attached, shown in the Additional Images section, ensuring that the voltage levels remain within the safety ratings of the op-amp.

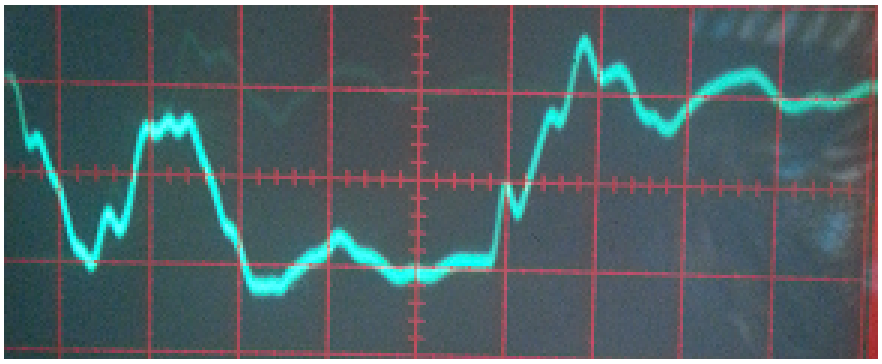


Figure 25: $(H1C - H2C)$ with $R_p = 500\ \Omega$, $R_a = 0\ \Omega$, $C = 15$ pF for the ICX424Q with two image sensors attached for the ICX424Q.
Vertical axis: 5V/div; Horizontal axis: 20ns/div; 0 volt line centered with vertical tick marks.

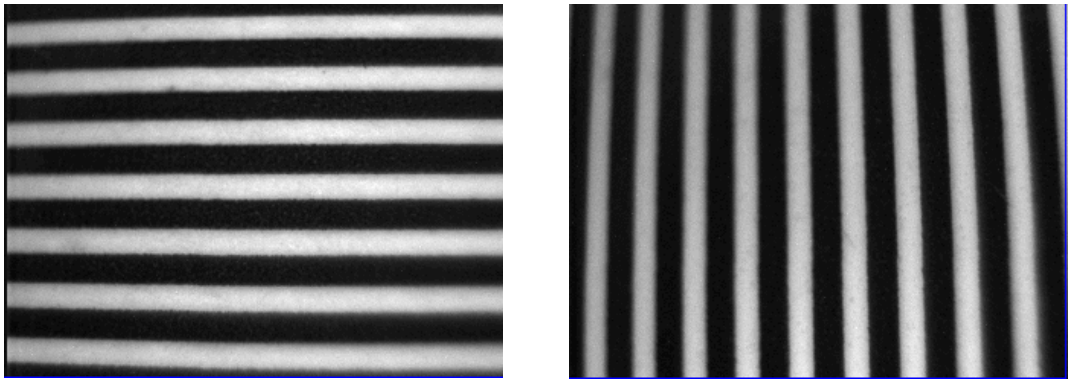


Figure 26: ICX424Q test images with $R_p = 500\ \Omega$, $R_a = 0\ \Omega$, and $C = 15$ pF.

Proposed changes for *new* A3025 HBCAM boards are as follows:

1. Remove all existing 47 Ω resistors: R40, R41, R42, R43.
2. Add 15 pF capacitors in parallel with the resistors R10, R12, and R14 in the feedback loops of the op-amps U7 and U10.
3. Add 500 Ω of resistance (two 1000 Ω resistors in parallel) in series between:

   Pin 38 of U5 and pin 5 of U7

   Pin 39 of U5 and pin 3 of U7.

   Pin 26 of U5 and pin 3 of U10.

Recommended changes to the *existing* A3025 HBCAM boards are as follows:

1. Replace R40, R41, R42, and R43 with 10 Ω resistors.
2. Add 15 pF capacitors in parallel with the resistors R10, R12, and R14 in the feedback loops of the op-amps U7 and U10.

Additional Images

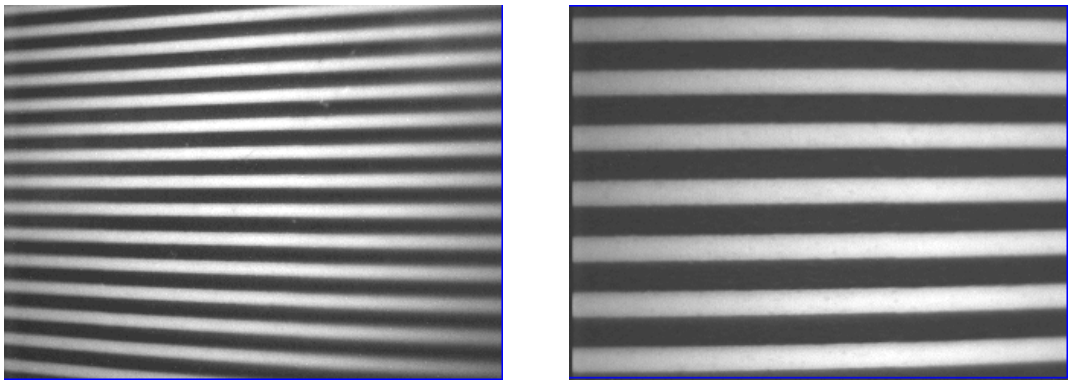


Figure 27: ICX424Q test images with a $R_a = 22\ \Omega$ (left) and $R_a = 47\ \Omega$ (right).

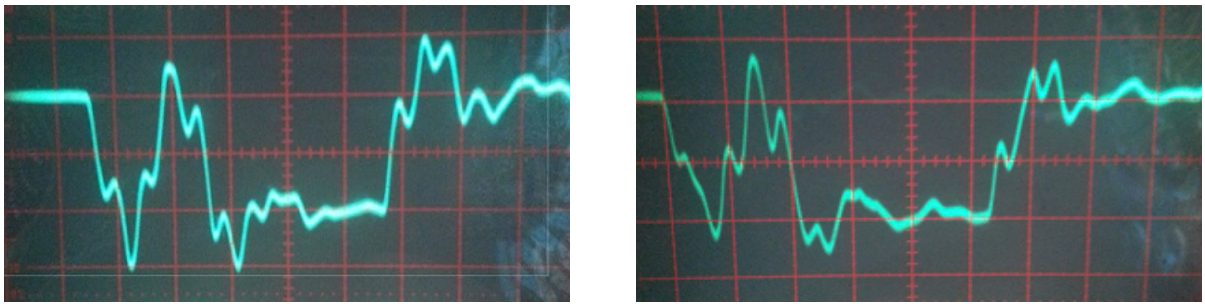


Figure 28: Left: $(H1C - H2C)$ with $R_p = 0\ \Omega$, $R_a = 10\ \Omega$, and $C = 15$ pF for ICX424Q with *one* image sensor attached. Right: $(H1C - H2C)$ with $R_p = 500\ \Omega$, $R_a = 0\ \Omega$, and $C = 15$ pF for ICX424Q with *one* image sensor attached.
Vertical axis: 5V/div; Horizontal axis: 20ns/div; 0 volt line centered with vertical tick marks.

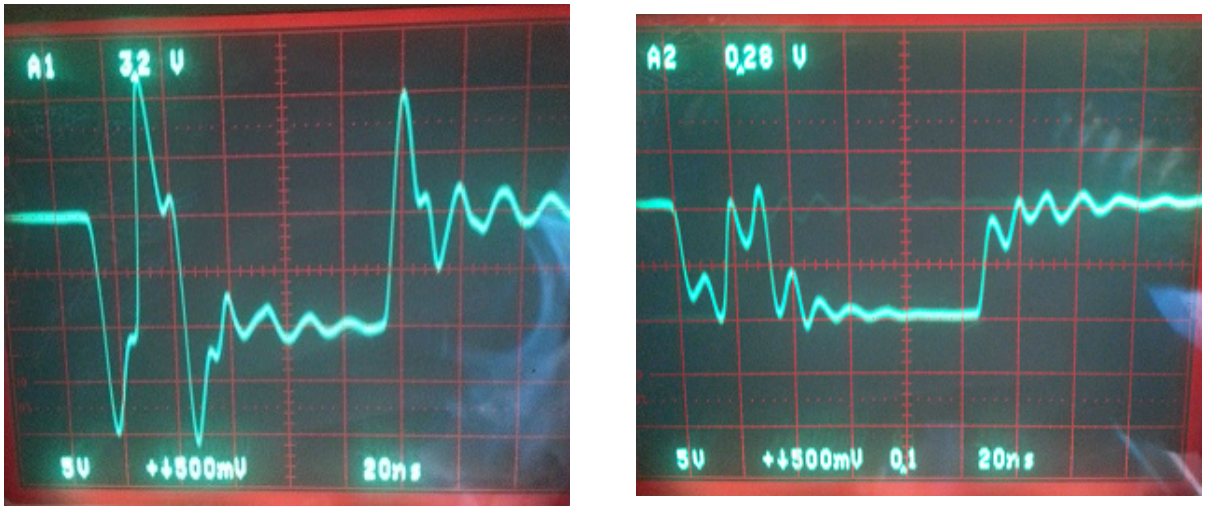


Figure 29: Left: $(H1C - H2C)$ with $R_p = 0\ \Omega$, $R_a = 10\ \Omega$, and $C = 15$ pF for ICX424Q with *no* image sensors attached. Right: $(H1C - H2C)$ with $R_p = 500\ \Omega$, $R_a = 0\ \Omega$, and $C = 15$ pF for ICX424Q with *no* image sensors attached.
Vertical axis: 5V/div; Horizontal axis: 20ns/div; 0 volt line centered with vertical tick marks.

Appendix

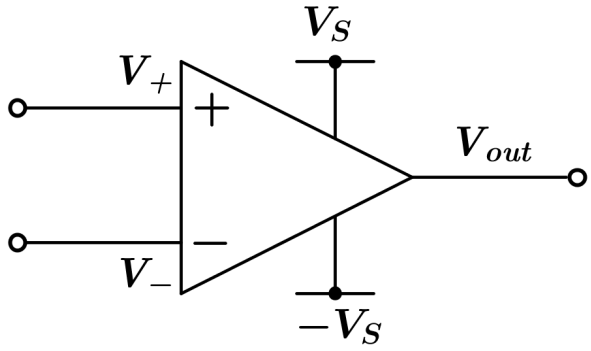
Operational Amplifiers

An operational amplifier (op-amp) is often used to amplify voltages within an electronic circuit. They have two inputs, typically marked + for the non-inverting input and − for the inverting input, and an output based on the difference in voltages of the inputs. This difference is often called the *differential input voltage* and is amplified by an extremely large gain, ranging from a hundred thousand to over a million. When the non-inverting input (+) is more positive than the inverting input (−), the output is positive and vice versa. The output of an op-amp is given by

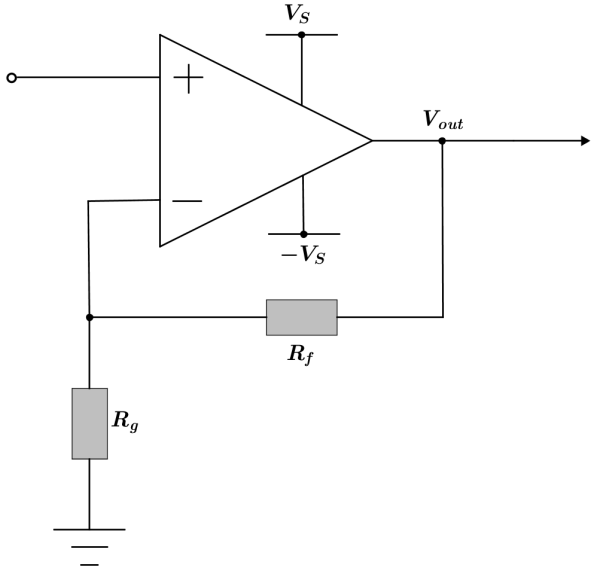
$$V_{out} = A(V_+ - V_-), \tag{5}$$

where A is the open-loop gain (no feedback) and V_+ and V_- are the inputs (see Figure 30). Op-amps can be used as comparators with no feedback, though they have far more applications with feedback *because* of their massive open-loop gain, as the output generally depends solely on the feedback network of the op-amp. Op-amps are designed such that in the ideal case with feedback:

1. The output is adjusted until the inputs are driven to the same voltage.
2. The inputs draw no current.



(a) Circuit diagram of an op-amp.



(b) Schematic of a non-inverting op-amp.

Figure 30: Circuit diagrams of op-amps.

One such example is in a non-inverting amplifier (Figure 30b), whose feedback network consists of a voltage divider that greatly reduces the gain. The output is pulled down until V_- matches that of V_+ and equilibrium is reached. Because the inputs draw no current, the current, I, through R_f and R_g is the same and

$$V_{out} = I(R_g + R_f) \quad \text{where} \quad I = \frac{V_+}{R_g}. \tag{6}$$

For an input voltage $V_{in} = V_+$, then, we have

$$\boxed{V_{out} = V_{in}\left(\frac{R_g + R_f}{R_g}\right) = V_{in}\left(1 + \frac{R_f}{R_g}\right).} \tag{7}$$

The feedback network used in the op-amps for the A3025 HBCAM boards includes a feedback capacitor in parallel with the feedback resistor (see Figure 20 where again, $V_{in} = V_+$). There no longer is a uniform current, but rather

$$I_{R_g} = I_{R_f} + I_C. \tag{8}$$

The above statement is equivalent to

$$\frac{V_-}{R_g} = \frac{V_{out} - V_-}{R_f} + C\frac{d(V_{out} - V_-)}{dt}, \tag{9}$$

but $V_- = V_+ = V_{in}$, so

$$\frac{V_{in}}{R_g} = \frac{V_{out} - V_{in}}{R_f} + C\frac{d(V_{out} - V_{in})}{dt}. \tag{10}$$

Re-arranging and grouping terms together, we have

$$V_{in}\left(1 + \frac{R_f}{R_g}\right) + R_f C\frac{dV_{in}}{dt} = V_{out} + R_f C\frac{dV_{out}}{dt}. \tag{11}$$

We are left with a differential equation with two different variables changing in time. However, we may overlook this when considering two cases of importance: an initially uncharged or charged capacitor with a constant input at time $t > 0$, for then $\frac{dV_{in}}{dt} = 0$ and equation (11) simplifies to

$$\frac{dV_{out}}{dt} = \frac{V_{in}\left(1 + \frac{R_f}{R_g}\right) - V_{out}}{R_f C}. \tag{12}$$

Let us consider the two cases separately, beginning with an initially low input that is switched on to high corresponding to an uncharged capacitor. Mathematically, this means $V_{in} = V_{out} = 0$ at time $t \leq 0$ and $V_{in} = V_0$ at time $t > 0$. Re-arranging equation (12), we have

$$\frac{dV_{out}}{V_{in}\left(1 + \frac{R_f}{R_g}\right) - V_{out}} = \frac{dt}{R_f C}. \tag{13}$$

Integrating both sides,

$$-\ln\left(V_{in}\left(1 + {}^{R_f}/_{R_g}\right) - V_{out}(t)\right) = \frac{t}{R_f C} + \alpha \tag{14}$$

and then exponentiating, absorbing the constant α into β,

$$V_{out}(t) = V_0\left(1 + {}^{R_f}/_{R_g}\right) - \beta e^{-t/R_f C}. \tag{15}$$

We can then solve for β by substituting our initial condition that $V_{out}(0) = 0$, yielding

$$\beta = V_0\left(1 + {}^{R_f}/_{R_g}\right). \tag{16}$$

Substituting into (15) and letting $V_{in} = V_0$ yields our familiar result, that

$$\boxed{V_{out}(t) = V_{in}\left(1 + \frac{R_f}{R_g}\right)\left(1 - e^{-t/R_f C}\right).} \tag{17}$$

The case where the input is initially high and is switched to low, corresponding to an initially charged capacitor, follows similarly. Here $V_{in} = V_0$ and $V_{out} = V_0\left(1 + {}^{R_f}/_{R_g}\right)$ at $t \leq 0$ and $V_{in} = 0$ at $t > 0$. The mathematics is identical until substitution of initial conditions and equation (15) becomes

$$V_{out}(t) = -\beta e^{-t/R_f C}. \tag{18}$$

Substituting $V_{out}(0) = V_0\left(1 + {}^{R_f}/_{R_g}\right)$, we have

$$\beta = -V_0\left(1 + {}^{R_f}/_{R_g}\right), \tag{19}$$

and resultantly

$$\boxed{V_{out}(t) = V_{in}\left(1 + \frac{R_f}{R_g}\right)e^{-t/R_f C}.} \tag{20}$$

References

[1] *Brandeis University High Energy Physics Electronics Shop.* <alignment.hep.brandeis.edu> 1 September 2013.